Akshat Ramachandran

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EDUCATION

Georgia Institute of Technology, Atlanta, GA **Aug 2023 – Present**
Master of Science in Electrical and Computer Engineering

Veermata Jijabai Technological Institute (VJTI), Mumbai, India **Aug 2018 – May 2022**
Bachelor of Technology in Electronics Engineering ***GPA: 9.80/10 (Gold Medallist)***

- **Thesis:** Next Generation Architecture for Computer Vision
- **Advisor:** Prof. John L. Gustafson (Arizona State University)

EXPERIENCE

Georgia Institute of Technology, Atlanta, GA **Jul 2023 – Present**
Graduate Research Assistant, Synergy Lab (Advisor: Dr. Tushar Krishna)

- Conducting research on accelerators and interconnection networks for on-chip platforms targeting AI workloads.
- Implementing a dataflow and arithmetic adaptive sparse matrix accelerator using HLS, outperforming SoTA by 5x.

Lemurian Labs, Toronto, Canada **Jun 2023 – Aug 2023**
Hardware Intern (Remote) (Managers: Mr. Ashish Kaul & Dr. Theodore Omtzigt)

- Designed and verified a smart NoC to interlink functional units in the Lemurian tensor engine using System Verilog and Python/PyUVM, achieving a 35% increase in operating frequency and 2.5x better performance over CONNECT NoC.
- Spearheaded cross-functional efforts to deploy Adaptive Logarithmic datatype in Python, C++ and assess mixed precision quantization of NumPy-implemented BERT and GPT, yielding a 10x speedup over floats.

Samsung Research & Development, Bangalore, India | Suwon, Republic of Korea **Aug 2022 – Jul 2023**
Visual Intelligence Engineer, XR & MX Group (Managers: Mr. B.V. Vandrotti & Mr. Jooyoung Kim)

- Involved in the accelerator/algorithm co-design, optimization and research-to-commercialization of depth perception, processing solutions for XR devices, securing ICIP publication, A2 patent and Samsung Best Paper Awards nomination.
- Co-designed and cross-validated a DL-based ToF Depth Fusion algorithm and SoC architecture in Python and HLS, enabling a 67% reduction in on-device inference latency over previous iterations.
- Designed a systolic dataflow accelerator in System Verilog for ToF acquisition, reducing latency from 120ms to 48ms.

Indian Institute of Technology, Bombay (IIT-B), Mumbai, India **Jul 2021 – Dec 2022**
Research Assistant, VLSI Lab (Advisor: Madhav P. Desai)

- Designed and verified a reconfigurable, programmable, and multi-thread 40-Gb/s NIC and MAC architecture in HLS, Verilog interfaced as a memory-mapped peripheral to the 2 × 4 × 32 Ajit processor. MeiTY funded project.
- Implemented custom packet generation & forwarding (for verification) and NIC support-software libraries in C.

Samsung Research & Development, Bangalore, India **May 2021 – Jul 2021**
Summer Research Intern, AR Vision Lab (Manager: Mr. Ankit Dhiman)

- Researched memory-efficient DL algorithms and architectures for AR applications.
- Remodelled Samsung's 3D reconstruction DL pipeline in Python, C and designed a memory controller that extrapolates the concept of k-means to parameters, achieving a performance boost of nearly 2× over existing pipelines.

TECHNICAL SKILLS AND QUALIFICATIONS

- **Research Interests:** HW/SW Co-Design, Network-On-Chips, Computer Architecture, Computer Vision, Deep Learning
- **Languages/Frameworks**: AHIR, Assembly, BlueSpec SystemVerilog, C/C++, CocoTB, CUDA, Keras, MATLAB, OpenCV, Python, SNPE, SPICE, TCL, Tensorflow, Verilog/System Verilog, VHDL, Vivado HLS (+ more)
- **Design Tools:** Android Studio, gem5, GNS3, ModelSim, MultiSim, PSpice, Quartus Prime, Xilinx Vivado (+ more)
- **Certifications & Training:** Design, simulate semiconductor devices, FPGA-based embedded systems, Deep learning, Advanced data structures and algorithms, Digital circuit design and analysis, ASIC design and verification
- **Relevant Coursework:** Computer Architecture, Digital/Analog Integrated Circuits, Image processing, VLSI design

PATENTS AND PUBLICATIONS (for a full list please see my Google Scholar page)

- **Ramachandran, A.**, Dhiman, A., Vandrotti, B.V., Kim., J. **Ntrans-Net: A Multi-Scale Neutrosophic Uncertainty Guided Transformer Network for Depth Completion.** *30th IEEE International Conference on Image Processing (ICIP), October 2023.*
- Ansari, R.A. and **Ramachandran, A. GPU-based building footprint identification utilizing self-attention multiresolution analysis.** *All Earth, Volume 35, Issue 1, April 2023.*
- **Ramachandran, A.**, Dhiman, A., Vandrotti, B.V., Kim, J., Boregowda, L.R. **A Method and System for Acquiring, Processing and Monocular Depth Completion/Estimation of sparse time-of-flight(ToF) sensors.** *Provisional patent filed with the Indian Patent Office based on work at Samsung Electronics Co. Ltd., February 2023.*
- **Ramachandran, A.**, Gustafson, J., Roy, A., Ansari, R.A., Daruwala, R. PositIV: **A Configurable Posit Processor Architecture for Image and Video Processing.** *25th Euromicro Conference on Digital System Design (DSD), August 2022.*

RELEVANT PROJECTS (for a full list please see my webpage)

Adaptive Compressed Sensing(CS) using posits **May 2022 – Dec 2022**

- Designed a configurable block-based CS architecture that jointly explores and adapts sampling rate and quantisation according to data characteristics.
- Developed a high-performance system architecture on FPGA using a generalised posits framework that achieves an average speed up of over 35× over other general-purpose architectures.

Colour Normalisation of Histopathology Images **Dec 2020 – Feb 2021**

- Designed a novel colour normalisation technique using multi-resolution neutrosophic sets to segment the individual stains in a tissue sample and perform landmark-based colour standardisation of each stain.
- Implemented the designed scheme in CUDA utilising adaptive patch samples for WSI images for real-time color normalisation.

NOTABLE HONORS AND AWARDS

- Recognized in the **top 5%** of advanced research in Samsung Electronics for my work on sparse ToF sensors towards the **Samsung Best Paper Award**. **Jun 2023**
- Received the **Samsung Spot Award** for outstanding contribution towards design and development of AR/VR algorithms and acceleration on Samsung Galaxy devices. **Sep 2022**
- Recognized for securing the **highest** cumulative **GPA** (out of 200 students) in the EE dept., VJTI and awarded the Dadabhai Naoroji Institute Gold medal. **Aug 2022**
- Won the **Best Undergraduate Thesis Award** in the EE dept. for the senior year project on **"Next Generation Architecture for Computer Vision"**. **Aug 2022**
- Awarded the Professional level SW Competency Certificate in the **Global Samsung Aptitude Test(GSAT)** at **Samsung Research, India** (acceptance rate = 30%). **Jul 2022**
- Secured the **second position** at **Electrothon Hackathon** for developing a disaster management application (in 48 hours) that aids in real-time and rapid disaster alleviation. **Mar 2022**
- Ranked **second** (out of 700 participants) for developing a DL model that achieves a precision of 90.27% for categorisation of post-earthquake satellite imagery at the **Vision Beyond Limits Competition**. **Dec 2021**
- Achieved **second** position (out of 1000 participants) in the **E-yantra International Robotics Competition** for designing a redressal robot on an FPGA to address threats in Industry 4.0. **Apr 2021**

TEACHING AND VOLUNTEERING

Program Committee, CoNGA'24, Singapore, Singapore **Aug 2023 – Present**

- Responsible for developing the conference's call for papers/abstracts, conduct peer review along with deciding the conference program with other members as part of the Conference on Next Generation Arithmetic 2024.

Teaching Assistant (Microprocessor Systems Lab), VJTI, Mumbai, India **Sep 2021 – Dec 2021**

- Aided Prof. Rohin Daruwala by teaching a class of 75 students on basics of digital system design and FPGA programming using Verilog HDL. Responsible for preparing and evaluating programming assignments.