Algorithm-Hardware Co-Design of Distribution-Aware Logarithmic-Posit Encodings for Efficient DNN Inference

Akshat Ramachandran¹, Zishen Wan¹, Geonhwa Jeong¹, John Gustafson², Tushar Krishna¹ ¹Georgia Institute of Technology, ²Arizona State University

Georgia Tech.

Motivation



Uniform Quantization: Substantial distributional variance and orders of magnitude difference in DNN parameters causing significant quantization errors.

- Floating-Point Techniques: Fail to adapt to the tapered distribution of DNN parameters and use flat accuracy, have increased hardware complexity.
- Why Posits?: Posit-based representations outperform floats in DNN inference, offering improved dynamic range, higher accuracy, simpler exception handling and tapered accuracy. But still have complex hardware.
- Logarithmic Posits: A composite data type that blends the adaptability of posits with the hardware efficiency of LNS.

Logarithmic Posits (LP)

- $x\langle n, es, rs, sf
 angle = sign(p) imes 2^{2^{es} imes k + e sf} imes 2^{ulfx}$ \Rightarrow Parameterizations for incorporating distribution-aware properties:
 - ✓ Bits (n): Identify optimal precision for a DNN layer.
 - Exponent Size (es): Controls dynamic range.
 - ✓ Regime Size (rs): Controls distribution shape.
 - ✓ Scale Factor (sf): Adjusts distribution position.
 - Express standard fraction and exponent in the logarithmic domain as a unified fixed-point exponent of the power of two as 2^{ulfx}, where ulfx=e+f.

(Learn more about standard posits here!)

LPQ Framework Component Effectiveness





This work introduces LP, a new composite data type for dynamic adaptation in DNNs, and LPQ, a quantization framework optimizing LP parameters with genetic algorithms. The LPA architecture integrates LP in a systolic array, enhancing computational efficiency. Our co-design maintains model accuracy with <1% drop and improves performance and energy efficiency over existing alternatives.

This work was supported in part by CoCoSys, one of seven centers in JUMP 2.0, a Semiconductor Research Corporation (SRC) program sponsored by DARPA.

Algorithm: Genetic-Algorithm Based LP Quantization (LPQ) Framework



> Fitness Function:

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4

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llfr ¢16

Integer

Weight Buffer(WB)

PE PE

Unified LP Decoder

Encoder MODE

 $r_{r+1} e_{r+1} s_{r+1}$

uffer (OB)

 A novel global-local contrastive loss, combats overfitting to calibration data and prevents premature convergence by minimizing representational divergence of intermediate layers.

Hardware: Logarithmic-Posit Accelerator (LPA)

₽6

Bit

m

^{3it Unpack} ← m]e_m ↓lnf_m

Log - Linear Converter

Two's Complement

Align Fractions

m[5:4]lfr[5:4] lfm[3:2]lfr[3:2]

Two's Complement

 lf_{r+1}

 $lf_m = (1+f)$

ulfx (u_w)

(16-bits)

Regime (rw

(16-bits)

Sign (s_w)

(4-bits)

XOR₄

lf,

MUL Stage

Mixed-precision LP MAC

unit made entirely of

Domain expressed as 4

implemented as gates.

integer blocks.

Multiplication

bit addition.

Log-Linear

Linear

using

adders

adder building

in Loa

Converter

Domain Addition

2-bit

multiple

w: Weight, a: Activation, r: MAC from prev. PE, r+1: MAC from current PE, MODE: m = m₁m₀

- ✓ Also includes a compression loss that drives the optimization to identify lower bit widths.
- ✓ This combination of fitness function drives the genetic algorithm for layer-wise quantization.